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Complete If Known

Application Number	10/659585
Filing Date	September 10, 2003
First Named Inventor	Shunpei YAMAZAKI et al.
Group Art Unit	2813
Examiner Name	Heather Doty

Attorney Docket Number

0756-7196

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
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		Office ⁴	Number ⁴	Kind Code ² (if known)				

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
HD		Stanley Wolf "4.5.6.3 Contact-Hole and Via Filling with Selective Electroless Metal Deposition," Silicon Processing for the VLSI Era, Vol. 2, Process Integration, pp. 256-257	
HD		M. Hatano et al., "A Novel Self-Aligned Gate-Overlapped LDD Poly-Si TFT with High Reliability and Performance," IEDM 97, pp. S23-526	
HD		U.S. Patent Application Serial No. 10/245,701 entitled Semiconductor Device and Method of Manufacturing the Same filed 09/18/2002	

Examiner Signature	<i>Heather A. Doty</i>	Date Considered	10/3/05
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